WHAT IS CLAIMED IS:

1. A non-volatile semiconductor memory device, comprising:

a plurality of memory blocks having a plurality of memory cells each arranged in matrix of rows and columns;

a plurality of word lines provided corresponding to said rows in said memory cell respectively;

a plurality of bit lines provided corresponding to said columns in said memory cell respectively;

a data bus line transmitting a potential of said bit line;

a column select circuit electrically coupling one bit line selected from said plurality of bit lines in accordance with a column select result to said data bus line;

a reference memory block having a plurality of reference memory cells arranged in matrix of rows and columns;

a plurality of reference word lines provided corresponding to said rows in said reference memory cell respectively;

a plurality of reference bit lines provided corresponding to said columns in said reference memory cell respectively;

a reference data bus line transmitting a potential of said reference bit line;

a reference column select circuit electrically coupling one reference bit line selected from said plurality of reference bit lines in accordance with a column select result to said reference data bus line; and

a sense amplifier arranged corresponding to said data bus line and said reference data bus line, and amplifying a potential difference between said data bus line and said reference data bus line; wherein

said column select circuit precharges remainder of said bit lines in a non-selected state to a prescribed potential during a data reading period in which one of said plurality of bit lines is driven to a selected state, and

said reference column select circuit precharges remainder of said reference bit lines in a non-selected state to said prescribed potential during a data reading period in which one of said plurality of reference bit lines is

driven to a selected state.

2. The non-volatile semiconductor memory device according to claim 1, wherein

said reference column select circuit selects one of said plurality of reference bit lines in accordance with a column select signal, which is a decode result of a low order bit of a column address for selecting a column in said plurality of memory cells, and electrically couples the selected reference bit line to said reference data bus line.

3. The non-volatile semiconductor memory device according to claim 2, wherein

said reference column select circuit electrically couples the reference bit line in a non-selected state among said plurality of reference bit lines to a precharge potential, in response to a reset signal activated during a period in which said column select signal is inactivated.

4. The non-volatile semiconductor memory device according to claim 1, wherein

in a burst mode in which data is successively transferred by a burst length defined by a high order bit of a column address, said reference column select circuit

precharges a first reference bit line and said bit line corresponding to a next address designated in an ascending order to said prescribed potential during a data reading period in which a second reference bit line and said bit line corresponding to a start address designated in accordance with said column address are driven to a selected state, and

precharges said second reference bit line and said bit line corresponding to further next address designated in an ascending order in a data reading period in which said first reference bit line and said bit line corresponding to said next address are driven to a selected state.

5. The non-volatile semiconductor memory device according to

claim 1, further comprising a plurality of connection switching circuits arranged between each of said plurality of memory blocks sharing said reference memory block and said reference memory block, wherein

said plurality of connection switching circuits couple one memory block selected from said plurality of memory blocks corresponding to a column address to said reference memory block.

6. The non-volatile semiconductor memory device according to claim 1, wherein

said sense amplifier forms a sense amplifier band constituted with a first sense amplifier amplifying a potential difference between a first data bus line and said reference data bus line, and a second sense amplifier outputting a potential of a second data bus line, and

said non-volatile semiconductor memory device further includes

first data reading means for selecting and coupling said reference bit line and said bit line corresponding to a start address to said first data bus line and said reference data bus line respectively, and amplifying a potential difference between said first data bus line and said reference data bus line in said first sense amplifier in a mode in which a plurality of pieces of data are successively transferred, and

second data reading means for selecting and coupling said bit line corresponding to a subsequent address to said second data bus line, and outputting a potential of said second data bus line in said second sense amplifier.

7. The non-volatile semiconductor memory device according to claim 6, further comprising a connection switching circuit coupled between said column select circuit and said first and second data bus lines, wherein

said connection switching circuit electrically couples a bit line corresponding to said start address to said first data bus line in response to activation of a control signal generated based on said start address, and electrically couples a bit line corresponding to said subsequent address to said second data bus line in response to inactivation of said control signal.